



PRINTED CIRCUIT BOARDS
INTERCONNECTION CARRIERS

State of the Art: PCB's		Revisio	Datum:	Seite:
PRINTED CIRCUIT BOARDS		01	4. 11. 2001	1/1
Schematic Key for Multilayer and HDI-Technology Built-Ups				
Registatur: C:\S_Daten\99_Archiv_Neutral\Multilayer_Aufbau_Doc\00p0e_KeyMultilayerBuilt-up 2003 09 01.doc				

a	b	c	d	e	f	g + h + i
04	188	FR4	55	L41.35_71.18	P10_20	v1.99_2-3_4-5_6-7_s0
columns and equal kind of positions are separated by "_". Equal prefixes in one column are reduced to one.						
04_188_FR4_L41.35_71.18_p10_20_v1.99_2-3_4-5_6-7_s0						

Parameter:		Examples	Explanation:	Units:	
a	numbers of layers:	core-layer	04	4-layer of MLBs	numeric
		sequential built-ups	(1-4-1)	2-outer-layer of sequential built-ups and 4-core-layer	
b	total thickness after the built up and final plating:	188	1880 μ	per 10 μ	
c	type of material:	FR4	quality of material		
d	copper thickness of the outer layer after the built up and final plating:	55	55 μ	per 1 μ	
e	different kinds of core material and copper foils on both sides:	L41.35_73.18	L = core material (prefix) p.e.: core thickness 410μ + cu foil 2 x 35μ + core thickness 730μ + cu foil 2 x 18μ	per 10 μ . per 1 μ	
f	number and thickness of the prepregs:	p10_20	p = prepregs (prefix) p.e.: core thickness 410μ + core thickness 730μ	per 10 μ	
g + h + i	buried vias:	v2-3	v = buried via (prefix) connects inner layer 2 to inner layer 3	inner layers	
	blind vias:	v1.99	v = blind via (prefix) connects outer layer 01 to inner layer 2/3/4 etc and outer layer 99 to inner 7/8 etc	outer layers: top outer is layer 1 and bottom outer is always layer 99 (p.e.: 4-layer ML has therefor layer 1+2+3+99)	
i	special code number of the assembly:	s0	none		
j	Standard-Multilayer:	<input checked="" type="checkbox"/>	default built-up in our factory	yes = <input checked="" type="checkbox"/>	
Tolerance on total thickness = +/- 5%. © Copyright by Printed Circuit Boards GmbH					