Art-Work - Film Preparation for Printed Circuit Board and Multilayer Boards

It doesn't take much to join the first group and get more involved with the board fabrication process. Run a series of checks and balances that help prepare the data set before sending it. Automated software is available to assist in this process, and all designers should at least do the following:

- Document layers and file names
- Take advantage of 274X
- Include IPC-D-356 netlist data
- Check spacing
- Identify potential drill problems
- Validate soldermask layers

First off, make sure layers are properly aligned and ordered correctly. File names should be meaningful, correlated with the layers, and explained to the fabricator in a README file. The idea here is that the fabricator should be able to quickly understand what each file is and where it goes in the stackup.

If you wish to continue using Gerber data, switch to 274X. 274D is obsolete; the external aperture information is more cumbersome and difficult for fabricators to deal with because they have to worry about translators and parsers to read the aperture table information. As a result, aperture data might be misinterpreted. Worse, someone might have typed in the information manually - and erroneously. By contrast, in 274X, all the aperture information is contained within the Gerber file, which can be read by most CAM tools automatically.

For netlists, IPC-D-356 is the preferred format for fabrication. It's widely used by many of the bare-board test-fixturing machines and is one of the only true ways to identify power-to-ground shorts. With the information in this format coming directly from the engineering CAD system, there's no danger of the fabricator "reverse engineering" the netlist from the Gerber files.

Next up are the internal plane layers. For some reason, CAD engineers like them to be "positive," but those types of layers lead to huge file sizes. Negative plane layers are usually preferred by fabricators because they're easier to work with and have smaller file sizes than positive layers. Remember, boards are manufactured en masse and must be stepped out into a panelized form. The result: Data sets with lots of unnecessary positive planes swell exponentially, bog down CAM systems, and crash photoplotters.

After the basic prep work is completed, step into the fabrication analysis arena, where the game is one of checks and balances. You've got your design rules; fabricators have theirs. Checks and balances can resolve any conflicts between the two.

| MicroCirtec Micro Circuit Technology GmbH mit Sitz in 47877 Willich |
| Registergericht: Amtsgericht Krefeld | Reg.-Nr.: HRB 2703 | Ust-Id-Nr.: DE 120 151 127 |
| Geschäftsführer: Hildegard Völker |
| Anschrift: 47805 Krefeld, Oberdiessemer Strasse 15 | Telefon: ++49 (0) 21 51 825 1 | Telefax: ++49 (0) 932 450 |

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Take soldermask layers, for instance. Often, these layers are not "intelligent" layers within a CAD tool; that is, there is not much in the way of capability checking within the tool. As a result, these are among the more troublesome layers for fabricators. The solution here is a fabrication analysis tool that can handle such issues as clearances, coverage, webbing, and so forth.

For instance, most fab shops want the largest possible clearances in a solder layer so that mask doesn't end up on pads. On the flip side, copper is not supposed to be exposed. The two requirements - no mask on pads and unwanted exposed copper - must be balanced. It is not easy to do. How can the designer help? Devise a standardized clearance, or set the clearances at 1:1, and let the shop do the soldermask enhancement.

Here's another issue: the soldermask webbing between pads on fine-pitch surface mount devices. Most masks can go to 0.003" without the resist flaking off. However, if the pads are so tightly grouped that the dams between them are less than 0.003", it's better to construct a mask opening over the entire group. That will make the fabricator's life much simpler.

Bear in mind that a fabricator's spacing tolerances likely differ from yours. For example, take the drill data. When laying out a board, you usually work with finished hole sizes. However, a fabricator must drill a hole larger than the finished one, about 0.004" to 0.005" over, then plate down to the desired finished size. This can lead to problems in maintaining annular ring requirements and copper spacing on internal layers. To meet manufacturing specs, the fabricator might have to modify the data, and that's the last thing you want.

So now we have an alternate reality: You've finished the PCB layout (check out those negative planes!). You output the 274X and IPC-D-356 netlist files. The data are fed into a fab analysis tool and run through their paces. Clearances are good. No possible soldermask flaking. Spacing between the drills is just right. You hand the data set to the fabricator, and voila! No unexpected phone calls, no changes in the layout, and the fabricator happily sends back a good set of boards on time.

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